New Ascon Implementations

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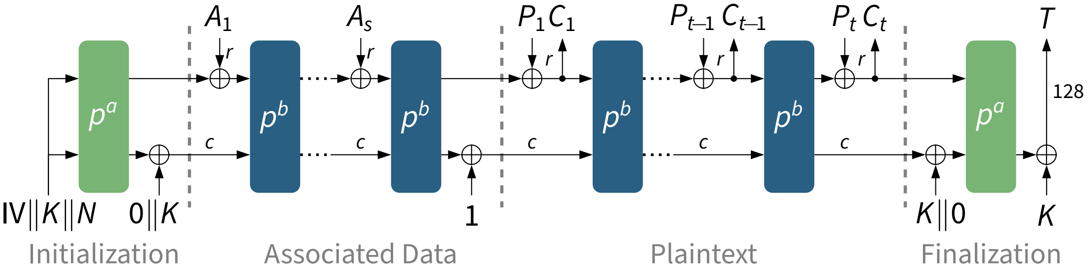
NIST LWC Workshop 2022

Outline

Ascon Overview

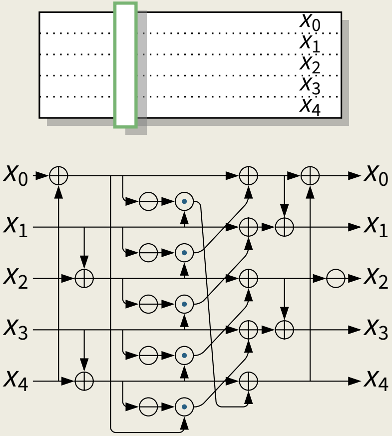
ASCON Mode for Authenticated Encryption



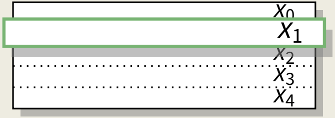
- Designed in 2014 [DEMS16], Journal of Cryptology in 2021 [DEMS21c]
- First choide for lightweight AEAD in CAESAR portfolio
- Extensive published cryptanalysis confirming its security margin
- Additional modes for Hash, XOF, MAC, PRF [DEMS21a; DEMS21b]

Ascon Permutation with $\{6, 8, 12\}$ Rounds

S-box layer



Linear layer



$$x_0 := x_0 \oplus (x_0 \ggg 19) \oplus (x_0 \ggg 28)$$

$$x_1 := x_1 \oplus (x_1 \ggg 61) \oplus (x_1 \ggg 39)$$

$$x_2 := x_2 \oplus (x_2 \ggg 1) \oplus (x_2 \ggg 6)$$

$$x_3 := x_3 \oplus (x_3 \ggg 10) \oplus (x_3 \ggg 17)$$

$$x_4 := x_4 \oplus (x_4 \ggg 7) \oplus (x_4 \ggg 41)$$

Ascon-128 vs Ascon-128a

- Ascon-128a: 33% more performance, more rounds, larger rate
- Same security, different trade-off (rate vs. number of rounds)
- Both scrutinized for 8 years in cryptographic competitions
- Most security analysis can be applied to both algorithms
- Similar security margin, no clear preference

Ascon Implementations

https://github.com/ascon/ascon-c (Ascon team)

- AEAD, Hash, XOF, MAC, PRF
- C: ref, speed/area optimized, combined
- ASM: esp32, armv6, armv6m, armv7m, rv32
- Masked C+ASM: 2-4 shares, leveled

https://github.com/rweather/ascon-suite (Rhys Weatherley)

- AEAD, Hash, HKDF, ISAP, KMAC, PBKDF2, PRNG, SIV, XOF
- 8/32/64-bit C, AVR, ARM, RISC-V, m68k, Xtensa (ESP32)
- Framework to generate C/ASM/masked implementations

Performance and Code Size

New Ascon Implementations

(Improvements in the Final Round)

- Fewer instructions for S-box [CJL+20]: -10%
- Improved 8-bit AVR [ascon-suite] (time/size): -11%/-44%
- Combined Ascon AEAD+Hash [ascon-c] (size): -17%
- Improved low-size [ascon-c] (size 128/128a/Hash): -7%/-30%/-20%
- Bit-interleaved interface [ascon-c] (time 128/128a/Hash): -17%/-23%/-5%
- ESP32 implementations [ascon-c][Bac22] (time/size): -66%/-64%
- RV32 implementations [ascon-c][Bac22] (RV32,RV32I,RV32B): New
- Masked ARMv6/RV32 [ascon-c] (leveled, 2-4 shares): New
- Ascon-Hasha, Ascon-Xofa [DEMS21b] (time): -33%
- Ascon-Mac, Ascon-Prf compared to Ascon-KMAC [DEMS21a] (time): -66%

Microcontroller Benchmarking

$\frac{ascon-nocrypt}{best-nocrypt}$ for primary submission @las3

Performance (time)		Code size (ROM)	
Uno:	1.34x	Uno:	3.22x
F1:	1.06x	F1:	1.62x
ESP:	1.92x	ESP:	1.31x
F7:	1.02x	F7:	1.10x
R5:	0.61x	R5:	1.07x

https://lwc.las3.de/ [2020/10/14]

Microcontroller Benchmarking

ASCON-128: best primary finalist in most categories

	Performance (time)	Code size (ROM)
Uno:	1.24x	1.59x
F1:	1.28x	0.80x
ESP:	0.58x	0.55x
F7:	0.89x	0.87x
R5:	0.55x	0.90x

https://lwc.las3.de/ [2022/05/05]

Microcontroller Benchmarking

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	Performance (time)	Code size (ROM)
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0-25% slower

https://lwc.las3.de/ [2022/05/05]

High-end Benchmarking

(Imagine Ascon hardware instructions)

AMD Ryzen 9:

- Ascon-128a: 5.1 c/b
- Ascon-128: 7.8 c/b
- Ascon-Hasha: 10.6 c/b*
- Ascon-Hash: 15.9 c/b

ARM Cortex-A72:

- Ascon-128a: 6.9 c/b
- Ascon-128: 10.4 c/b
- Ascon-Hasha: 13.5 c/b*
- Ascon-Hash: 20.2 c/b

https://bench.cr.yp.to/ [2022/05/03]

* estimated, not yet benchmarked

Implementation Techniques

Flexibility of Ascon Components

- Parallelism: S-box and linear layer support up to 5 ALUs
- Small state: 10 32-bit registers, 2 temporary, 1 for loop
- S-box: new description with fewer instructions
- Linear: 64-bit rotate or bit interleaving or funnel shift
- Modes: combine absorb, squeeze, insert (xor, read, write)
- Rate: loop for combined implementations (rate 64, 128)
- Short messages: only init and final needed

Ascon Hardware Extensions

- Fast, lightweight Ascon round instruction for 32-bit ARM/RV32 [SP20]
  - RI5CY Ascon-*p* with 4.7kGE: speedup factor 50x
  - Reuse 10 registers of CPU register file
- ARM Custom Datapath Extendion, RISC-V Bitmanip Extension, ...
  - 32-bit funnel shift instructions (RV32B: FSRI, ESP32: SRC)
  - 32-bit interleaving instructions (RV32B: ZIP/UNZIP, ARM CDE: CX3)
  - Fused AND/XOR, BIC/XOR instructions (ARM A64: BCAX, ARM CDE: CX3A)
  - SHA-2 like Sigma instructions (ARM CDE: CX3DA)

Bit-interleaved Interface

(ascon128bi32, ascon128abi32, asconhashbi32, asconhashabi32)

- Convention: data is stored/transmitted in bit interleaved format
- Communication parties need to agree, similar to endianess
- Improved performance on 32-bit ARM platforms:
  - Ascon-128/Ascon-128a: -17%/-23%
- Also demonstrates improvement of Ascon with
  - Bit-interleaving instructions (obvious)
  - Funnel shift instructions (same effect!)

Side-channel Protection

Designed with SCA in Mind

- Algebraic degree 2 of S-box
- Limited damage if state is recovered
- Leveled implementations [BBC+20]
  - Higher protection order for Init/Final (key)
  - Lower protection order for AD/PT/CT processing (data)
- Masking using Toffoli gate [DDE+20]

Masking using Toffoli Gate

- More efficient than masked AND gate
  - Fewer instructions, registers, randomness
- No fresh randomness needed during round computation
  - Randomness is not lost (invertible shared Toffoli gate)
  - Randomness of previous round can be reused
- Benefits of invertible shared function:
  - Uniform by design
  - SIFA: Reduced attack surface if used with redundancy [DDE+20]

1st-order Masked Keccak S-box

```
State:[a0,a1,b0,b1,c0,c1,d0,d1,e0,e1,r0]

(r1,r0) ← clone(r0)
toffoli_shared(r0,r1,e0,e1,a0,a1)
toffoli_shared(a0,a1,b0,b1,c0,c1)
toffoli_shared(c0,c1,d0,d1,e0,e1)
toffoli_shared(e0,e1,a0,a1,b0,b1)
toffoli_shared(b0,b1,c0,c1,d0,d1)
d0 ← xor(d0,r0)
d1 ← xor(d1,r1)
```

- Similar constructions for higher degree S-boxes may be less efficient [DDE+20]

Further SCA Optimizations

- Preliminary Goal: Achieve 1st-order protection with 2/3 shares in C[1]
  - Rotation offset between shares
  - Minimum number of ASM instructions (Toffoli gate)
  - Some register clears/NOPS needed
  - Extension to 3-shares with trick from [SM21]
- Performance in cycles/byte (green: evaluated)

impl/shares flags	armv6	C -O2	C -Os	2-1-2 -O2	2-1-2 -Os	2 -O2	2 -Os	3 -O2	3 -Os
ARM1176JZF	58	70	85	88	100	260	343	524	703
STM32F415	59	84	90	90	98	320	378	650	669

[1] Our implementations should be considered as a starting point to generate device specific C/ASM implementations

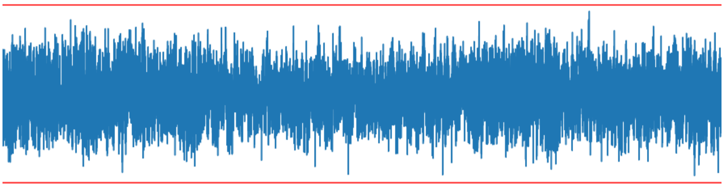
Evaluation and Verification

Testvector Leakage Assessment

- Goal: 1[st]-order protection with 2/3 shares
- Evaluation setup:
  - ChipWhisperer-Lite
  - UFO Board
  - `STM32F303`, `STM32F415`
  - We set $p^a, p^b = 2$ due to limited sample buffer
- We present decryption results of `protected_bi32_armv6`
- More implementations/results available at:
  https://github.com/ascon/simpleserial-ascon

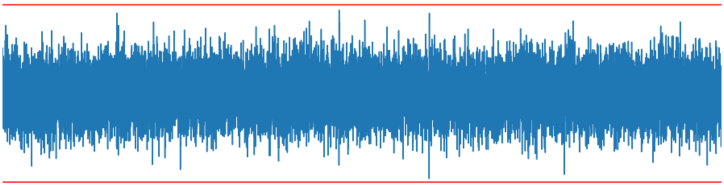
TVLA Results

- STM32F303
- 3 (rotated) shares
- No device-specific fixes
- 8m traces



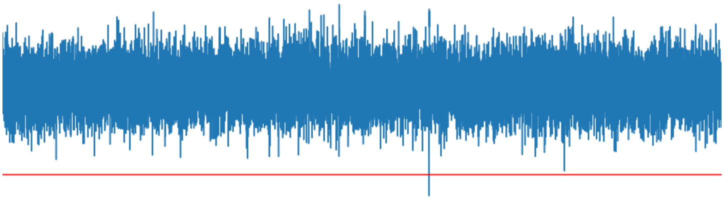
TVLA Results

- `STM32F415`
- 2 (rotated) shares
- Device-specific fixes
- 4m traces



TVLA Results

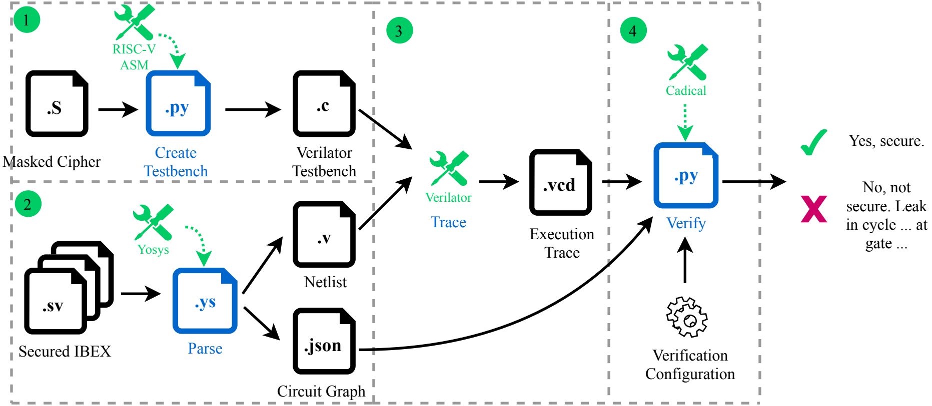
- `STM32F415`
- 2 (rotated) shares
- Device-specific fixes
- 5m traces



Formal Masking Verification

- Formal verification of masking in SW/HW using Coco [GHP+21]
  - Based on ideas of REBECCA [BGI+18]
- Verifies masked software in “hardware probing model” on CPU netlists
  - Considers stable signals, transitions, glitches
  - RISC-V IBEX core (comparable to ARM Cortex-M0)
- Also suitable for masked hardware circuits with/without state machines

Coco Verification Flow



Coco Verification Results

- Hardened RISC-V IBEX core from [GHP+21] as reference
- We mapped one round of 2-share ASCON-*p* round from to RISC-V ASM
- We verified 1st-order probing security (incl. transitions/glitches)
  - No online randomness
  - Performance of 260 c/b
  - Multi-round correctness due to uniformity of masking

Questions

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