A Comparative Study of Performance of AES Final Candidates Using FPGAs

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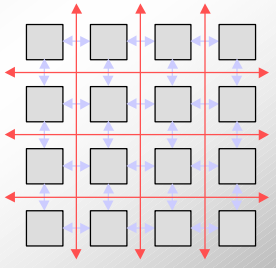
Outline

- Why FPGAs?
- Design decisions
- Results

FPGAs Overview

- Configurable hardware
  - programmable logic cells
  - programmable interconnection
  - can be reconfigured
- Performance crux
  - massive parallelism
  - hardware specialization
  - hardware reuse



Why FPGAs ?

	Low		High
Efficiency	µP	FPGA	ASIC
Flexibility	ASIC	FPGA	µP
Power	ASIC	FPGA	µP
Cost	FPGA	µP	ASIC

Design Decisions

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- Maximize time performance
- Metrics
  - throughput (bit/sec)
  - latency (key-setup)
- Encryption
  - 128-bit data block and key size

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“Single-round” Implementations

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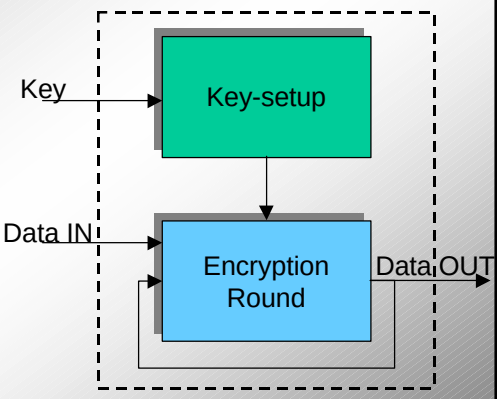
- Key-setup on-the-fly
  -

  Focus in algorithmic characteristics
  - parallelism at the round level
  -



t_{round}) bit/sec

n: # of rounds
t_{round} : encryption time per round

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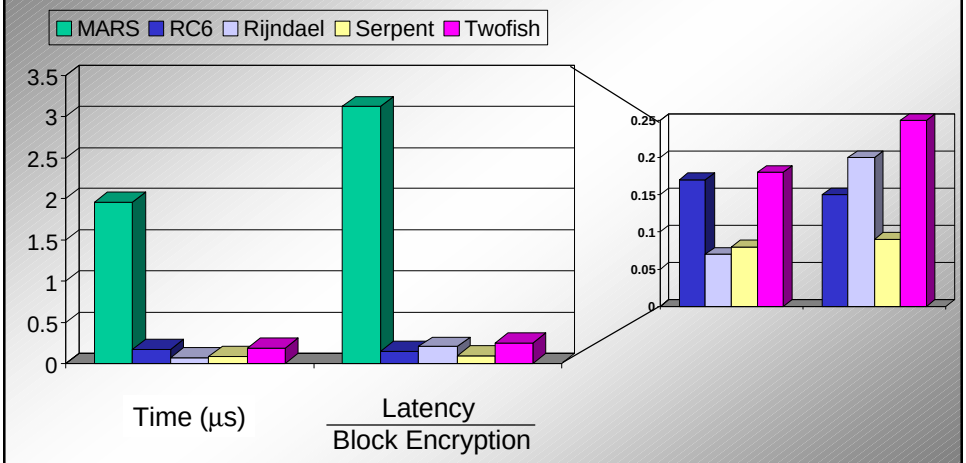
Hardware Target

- Xilinx VIRTEX FPGAs
  - speed -6
- Explore on-chip memory blocks
  - key-dependent data
    - sub-keys, S-boxes
- Software tool
  - Xilinx Foundation 2.1i
    - logic synthesis
    - place & route

Latency Results



Compared with NIST Efficiency Testing Round 1: 20 - 700x speed-up

Throughput Results

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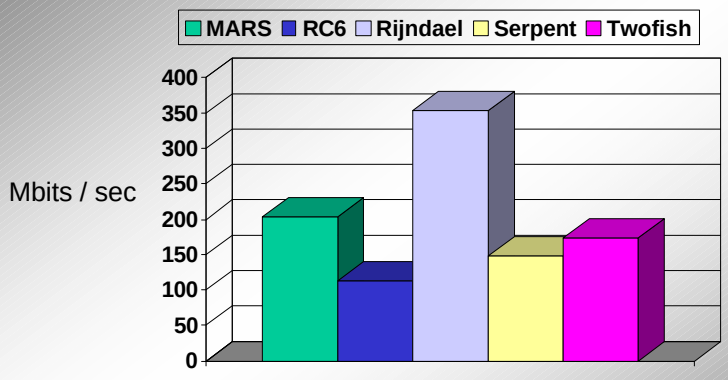

Compared with NIST Efficiency Testing Round 1: 4 - 20x speed-up

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Area Results

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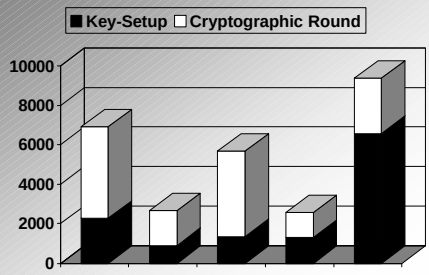
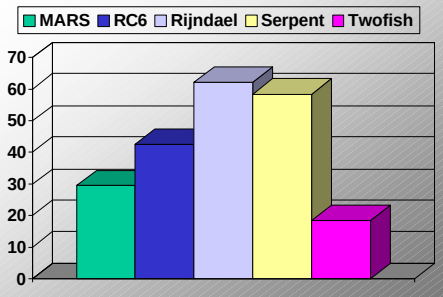


# of VIRTEX slices



Kbits/(sec*slice)

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Time Performance Summary

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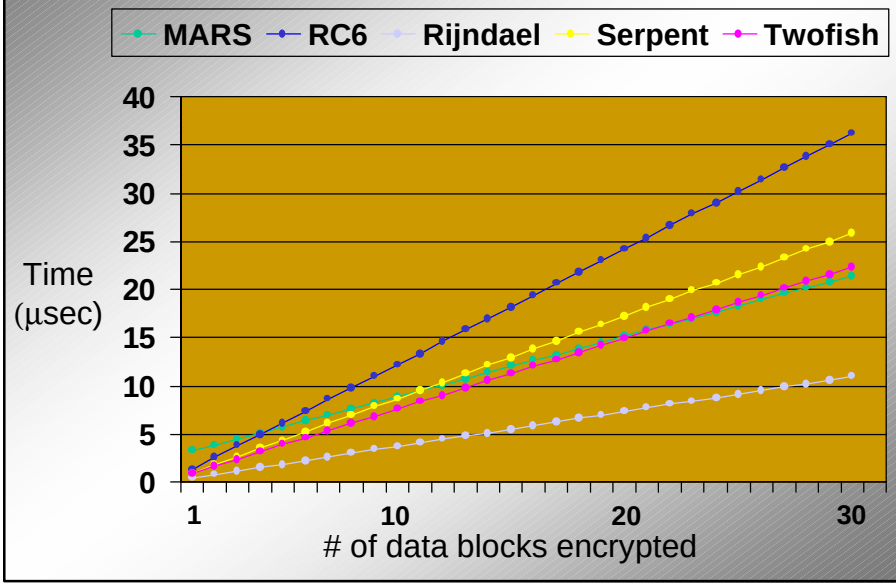

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Conclusions

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- FPGAs
  - hardware-like performance
  - software-like flexibility
- Latency/Throughput metrics
- Performance analysis can be extended
  - parallelism among rounds
  - relative comparisons in terms of …
- Which algorithm “fits” FPGAs the *best* ?
  - Rijndael, Serpent

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