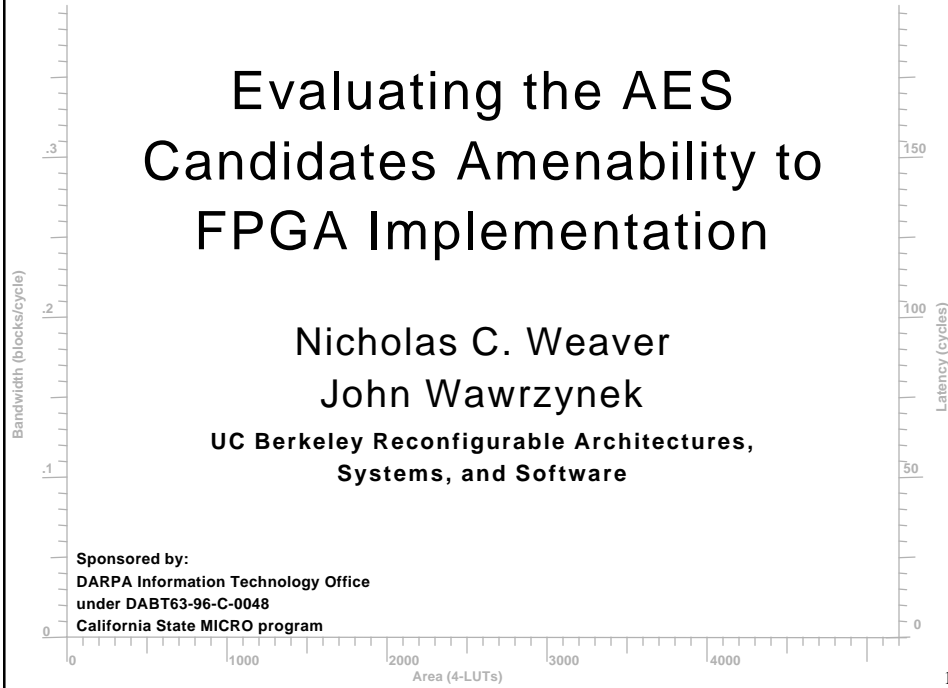


# Evaluating the AES Candidates Amenity to FPGA Implementation

Nicholas C. Weaver  
John Wawrzynek

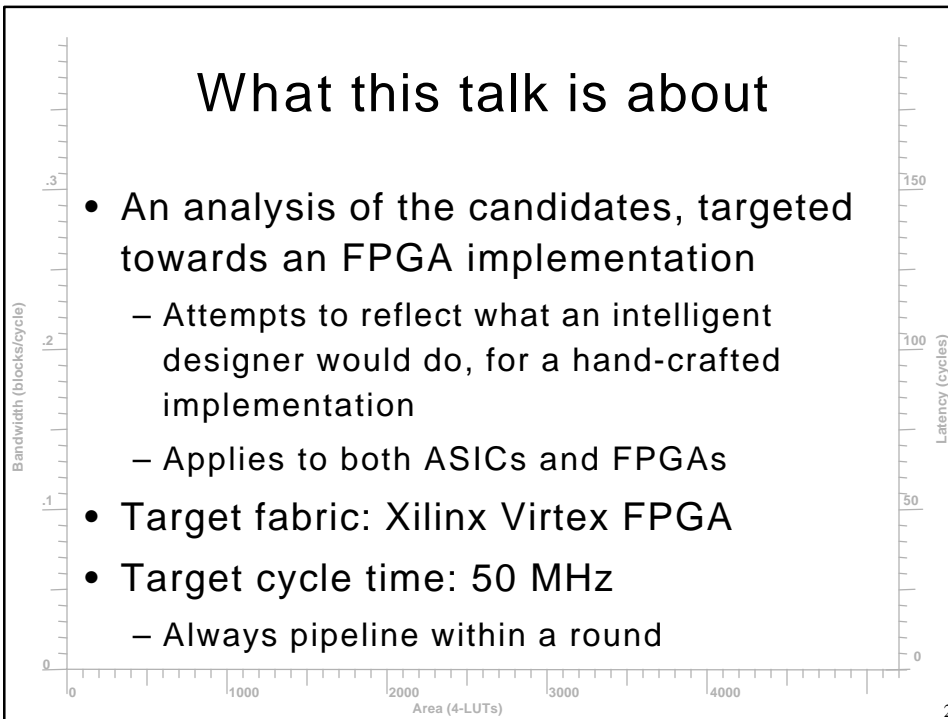
UC Berkeley Reconfigurable Architectures,  
Systems, and Software

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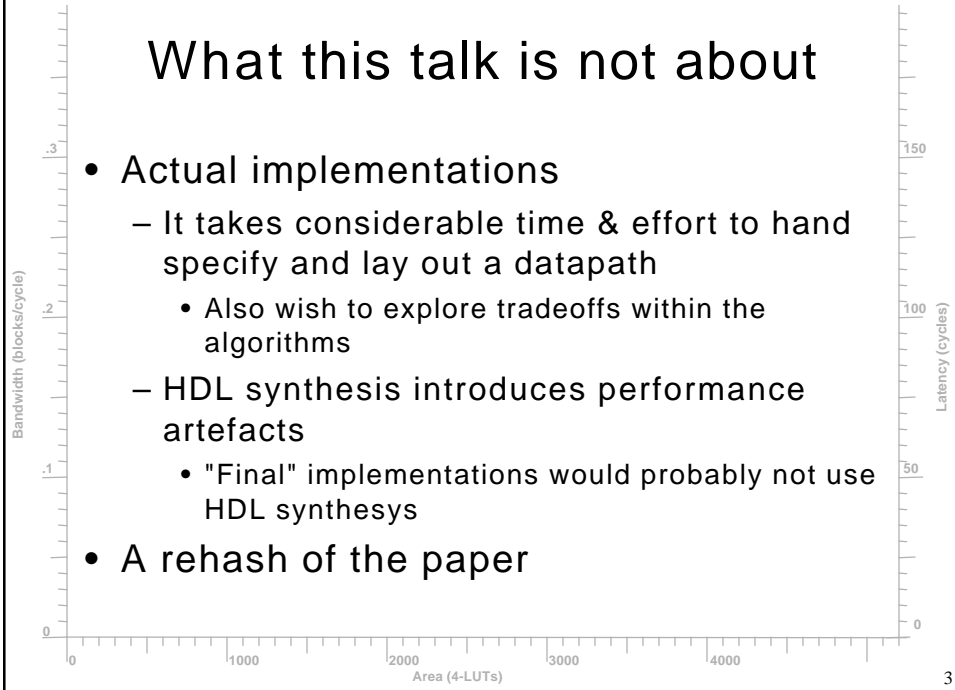
## What this talk is about

- An analysis of the candidates, targeted towards an FPGA implementation
  - Attempts to reflect what an intelligent designer would do, for a hand-crafted implementation
  - Applies to both ASICs and FPGAs
- Target fabric: Xilinx Virtex FPGA
- Target cycle time: 50 MHz
  - Always pipeline within a round



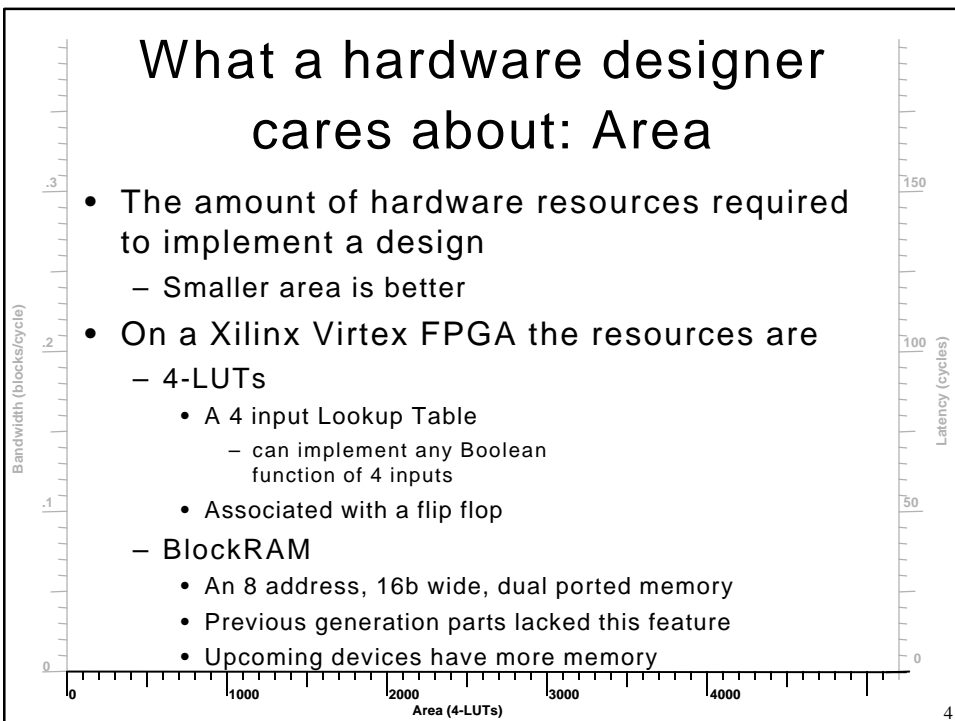
## What this talk is not about

- Actual implementations
  - It takes considerable time & effort to hand specify and lay out a datapath
    - Also wish to explore tradeoffs within the algorithms
  - HDL synthesis introduces performance artefacts
    - "Final" implementations would probably not use HDL synthesis
- A rehash of the paper



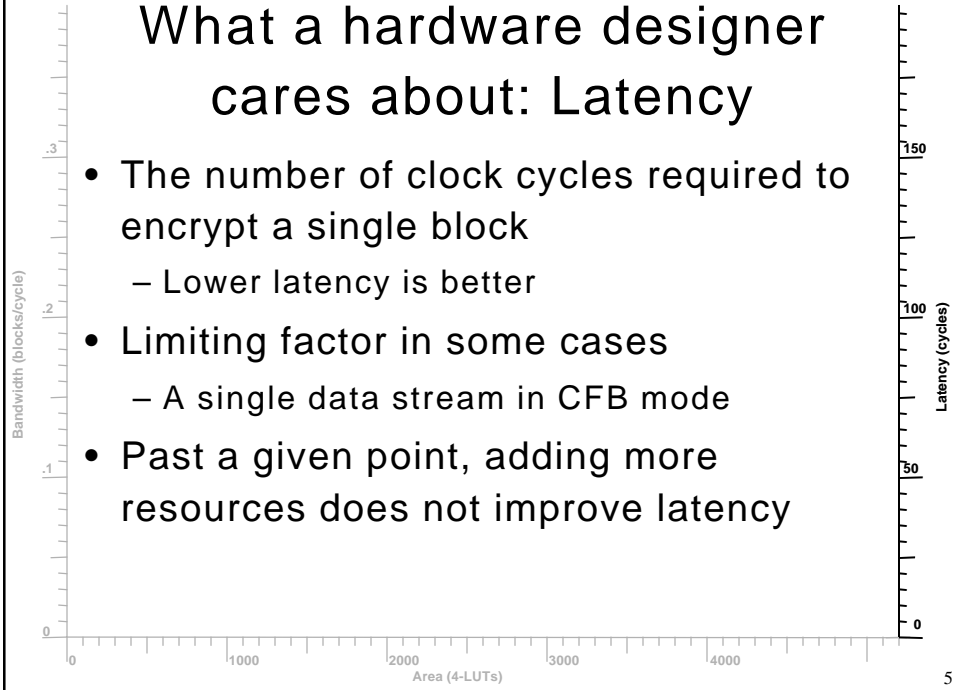
## What a hardware designer cares about: Area

- The amount of hardware resources required to implement a design
  - Smaller area is better
- On a Xilinx Virtex FPGA the resources are
  - 4-LUTs
    - A 4 input Lookup Table
      - can implement any Boolean function of 4 inputs
    - Associated with a flip flop
  - BlockRAM
    - An 8 address, 16b wide, dual ported memory
    - Previous generation parts lacked this feature
    - Upcoming devices have more memory



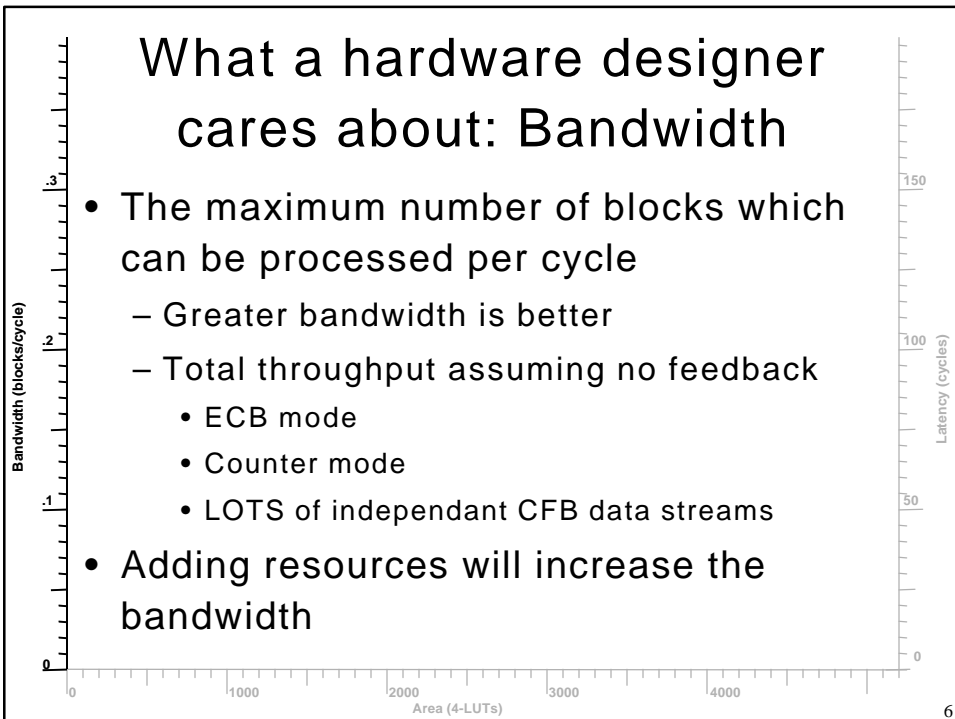
## What a hardware designer cares about: Latency

- The number of clock cycles required to encrypt a single block
  - Lower latency is better
- Limiting factor in some cases
  - A single data stream in CFB mode
- Past a given point, adding more resources does not improve latency



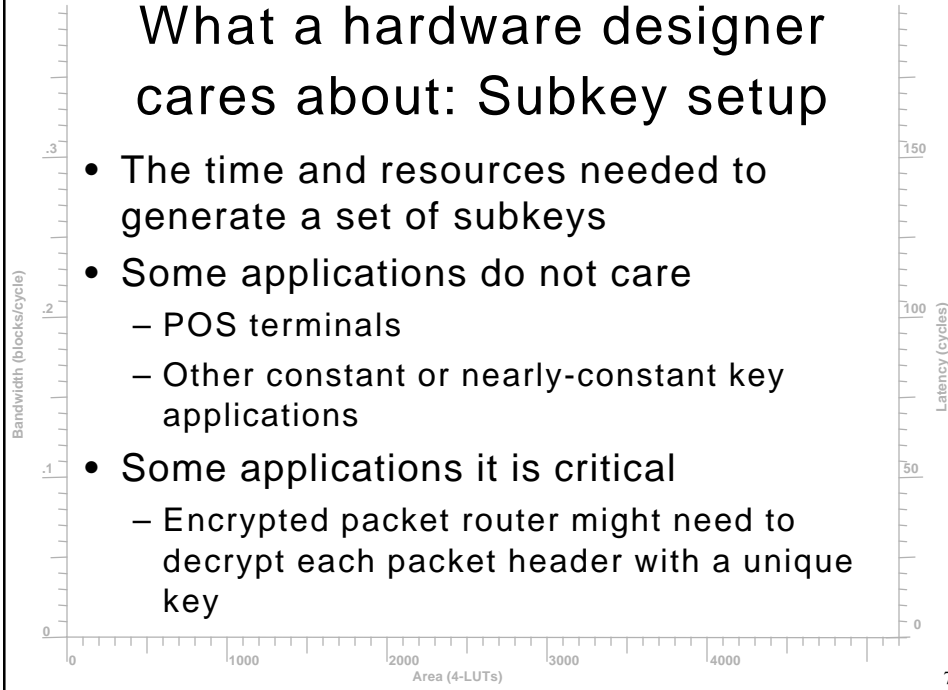
## What a hardware designer cares about: Bandwidth

- The maximum number of blocks which can be processed per cycle
  - Greater bandwidth is better
  - Total throughput assuming no feedback
    - ECB mode
    - Counter mode
    - LOTS of independant CFB data streams
- Adding resources will increase the bandwidth



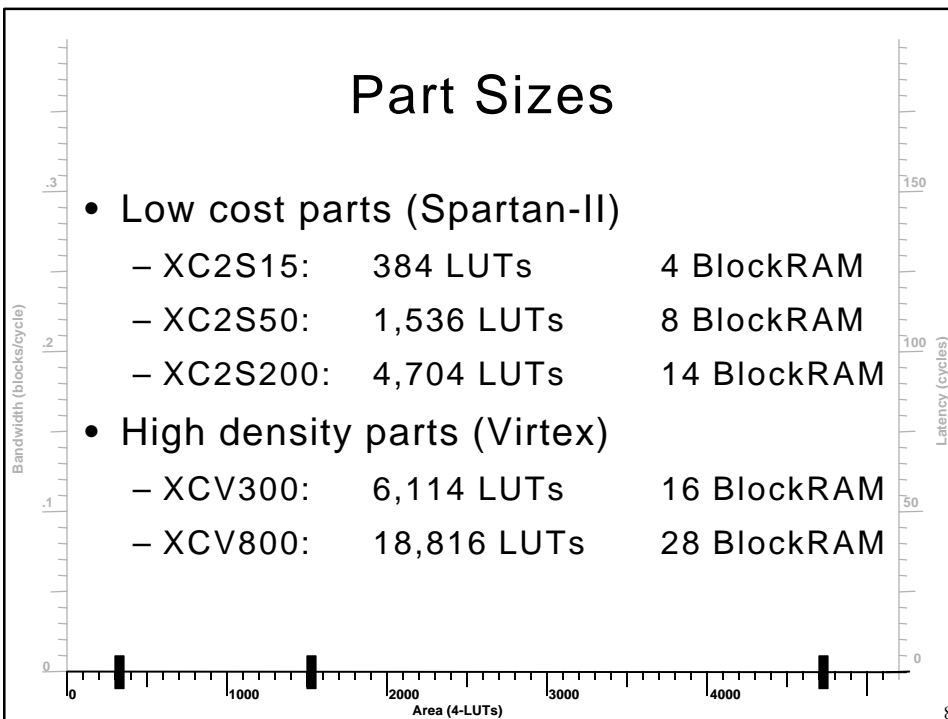
## What a hardware designer cares about: Subkey setup

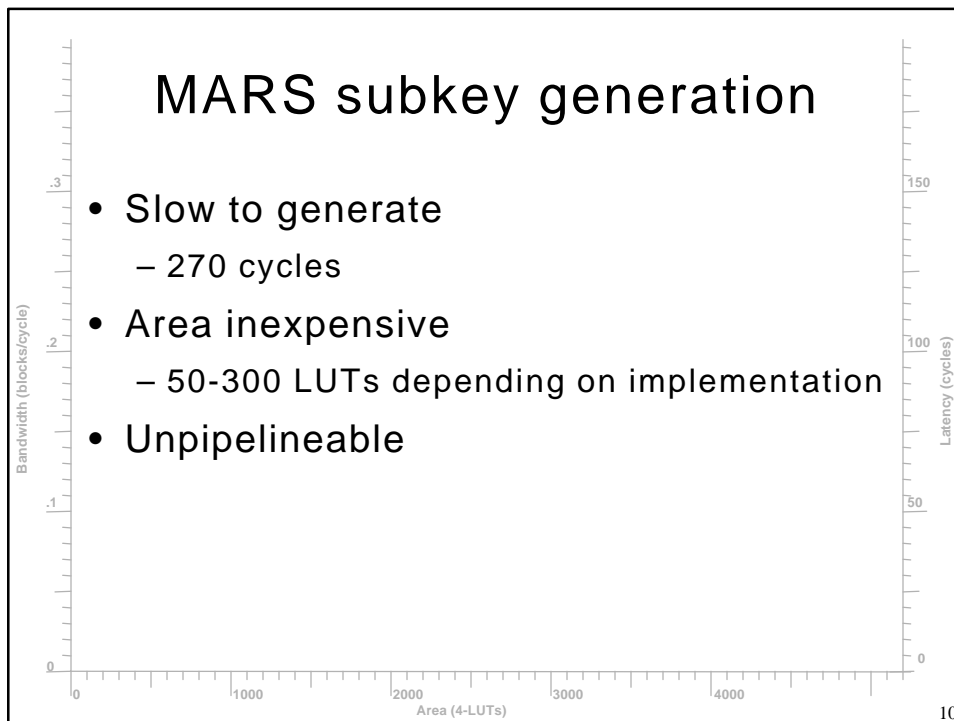
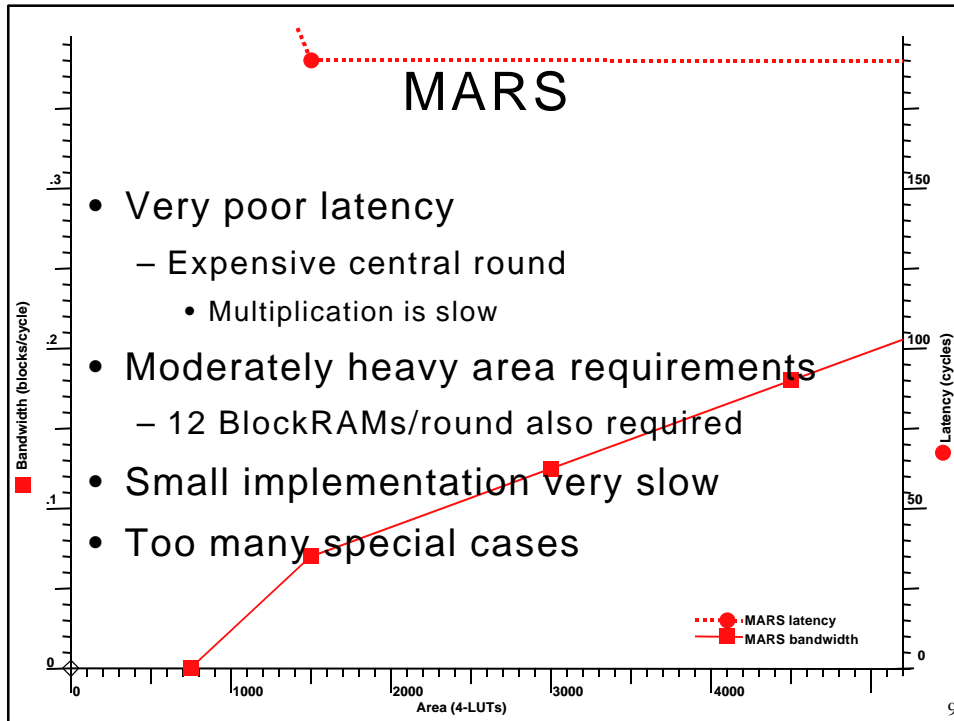
- The time and resources needed to generate a set of subkeys
- Some applications do not care
  - POS terminals
  - Other constant or nearly-constant key applications
- Some applications it is critical
  - Encrypted packet router might need to decrypt each packet header with a unique key

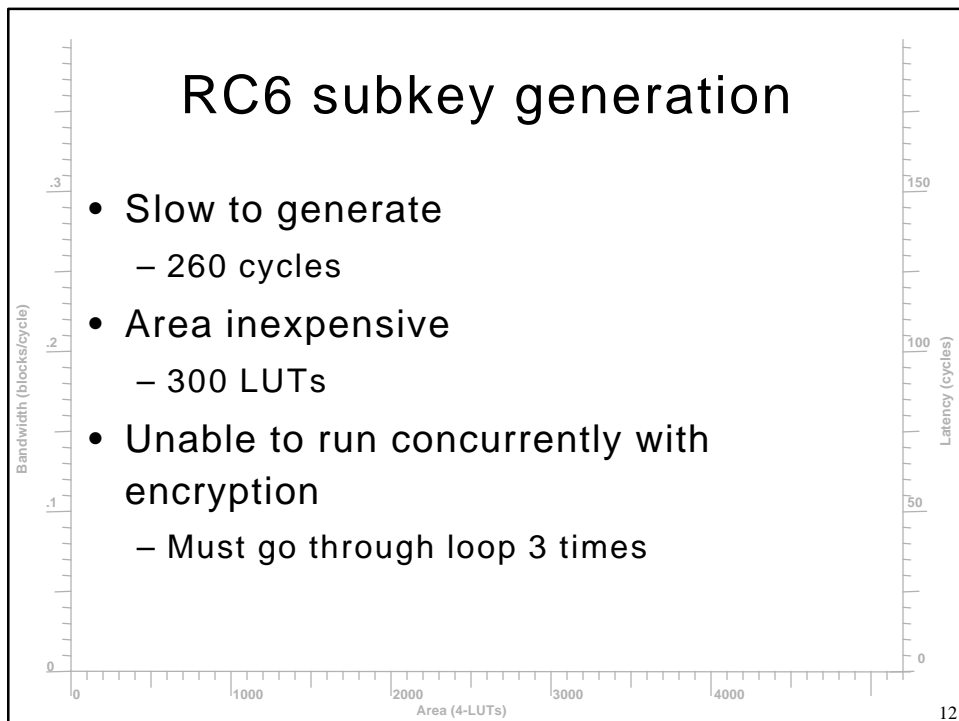
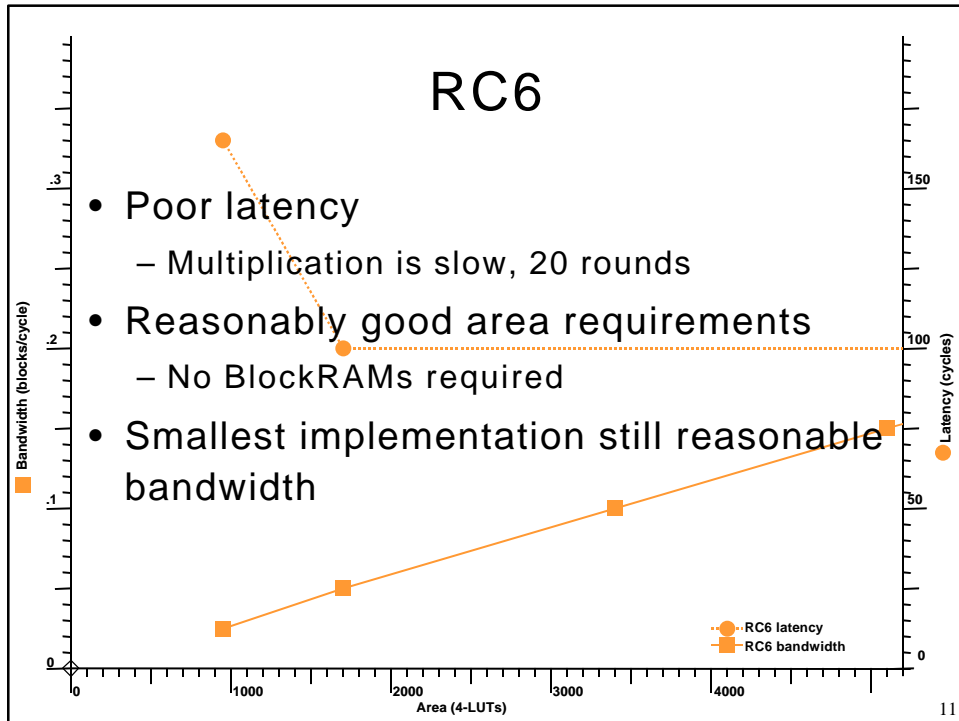


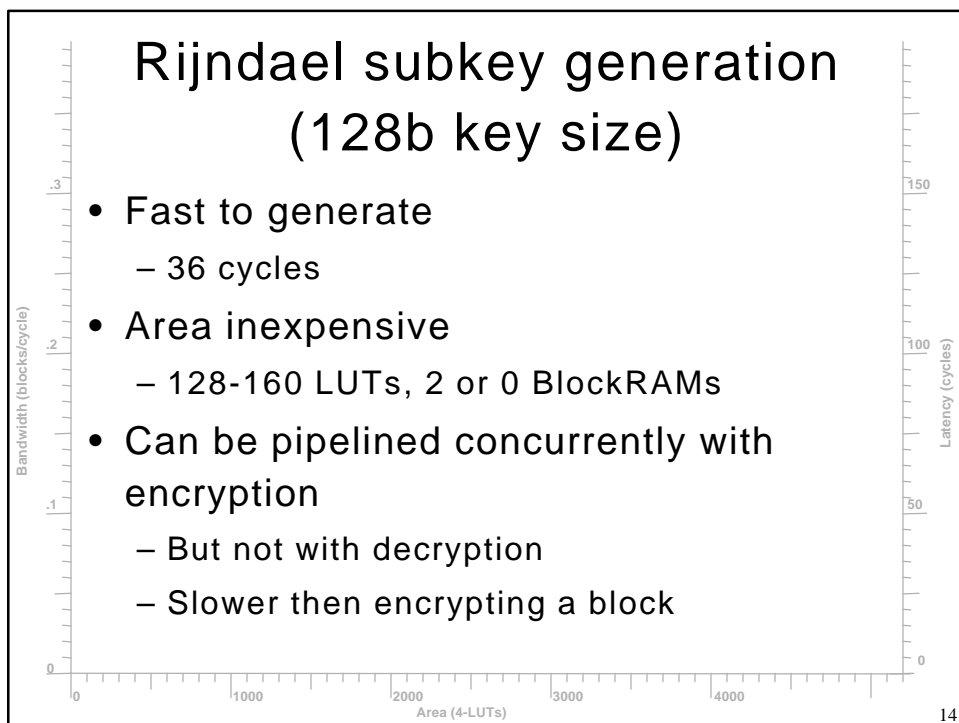
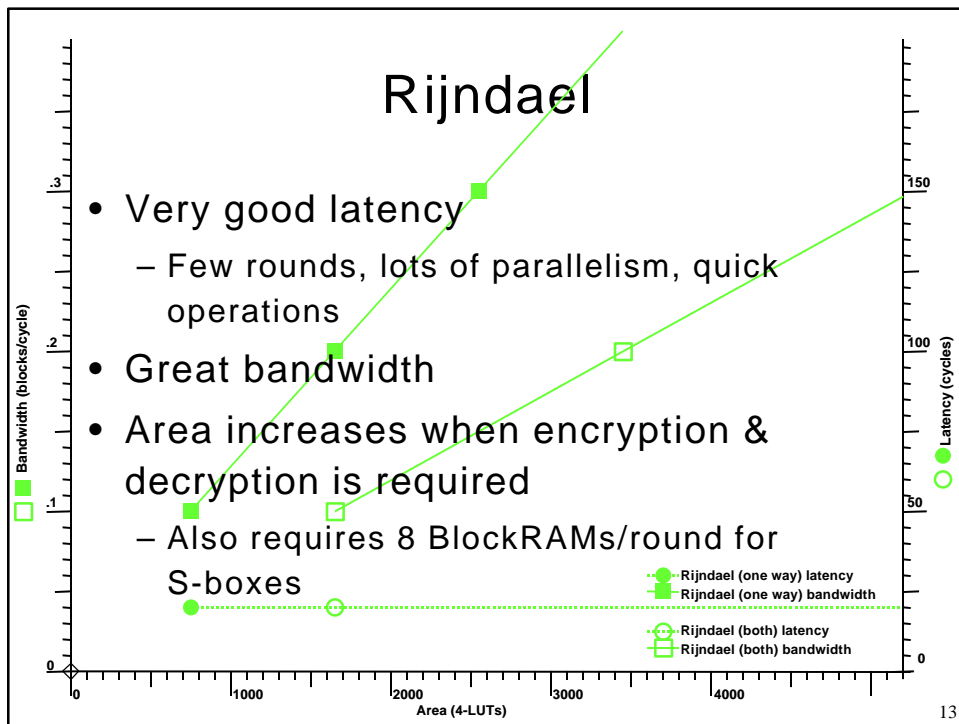
## Part Sizes

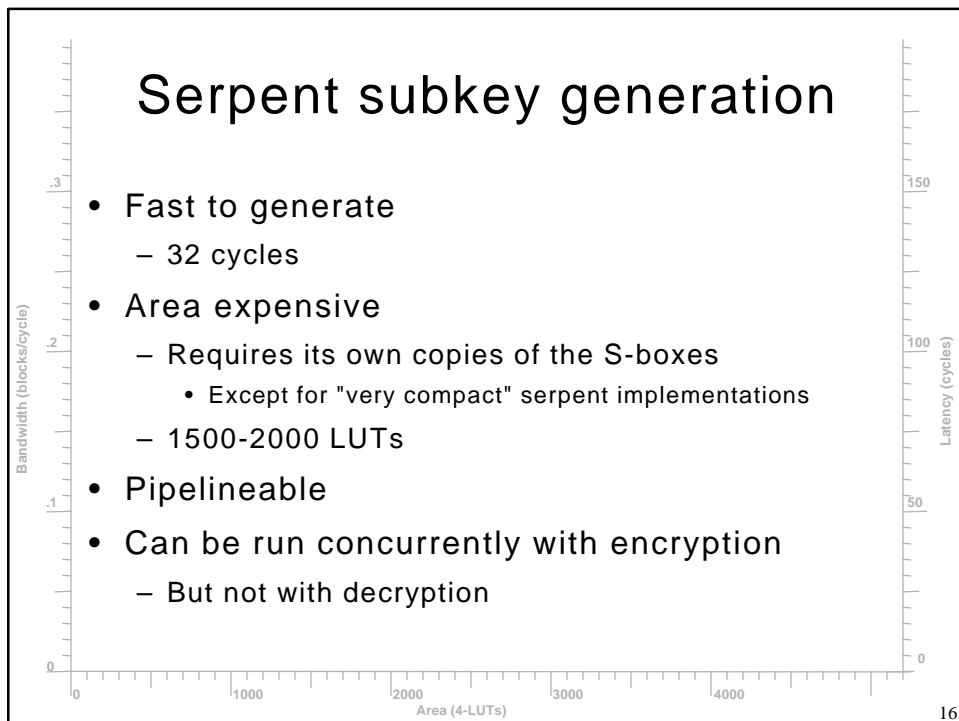
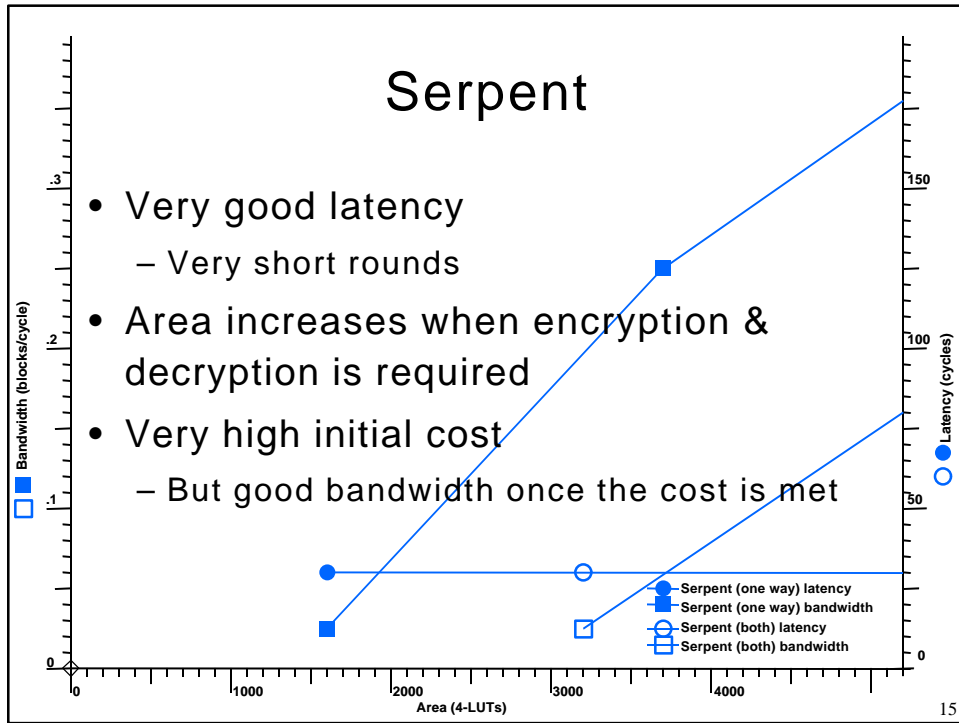
- Low cost parts (Spartan-II)
  - XC2S15: 384 LUTs 4 BlockRAM
  - XC2S50: 1,536 LUTs 8 BlockRAM
  - XC2S200: 4,704 LUTs 14 BlockRAM
- High density parts (Virtex)
  - XCV300: 6,114 LUTs 16 BlockRAM
  - XCV800: 18,816 LUTs 28 BlockRAM





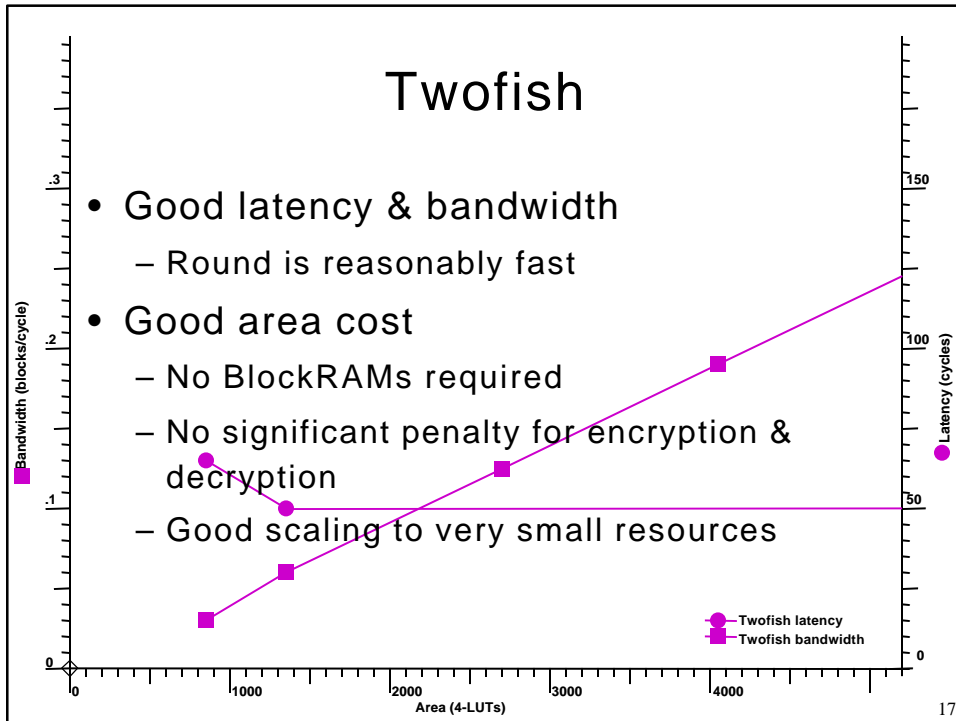




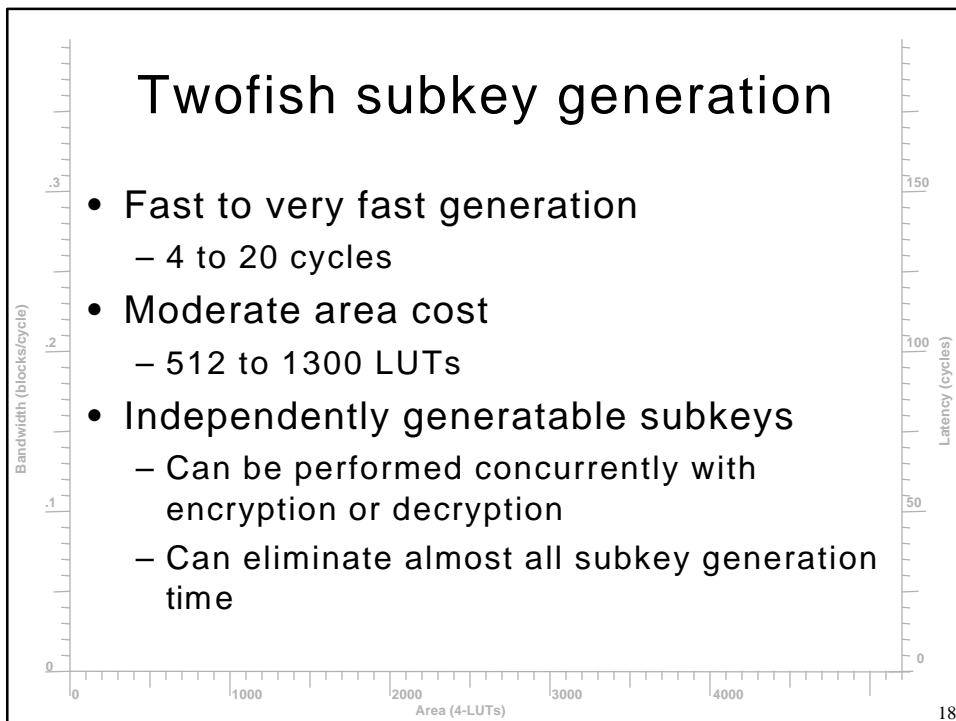


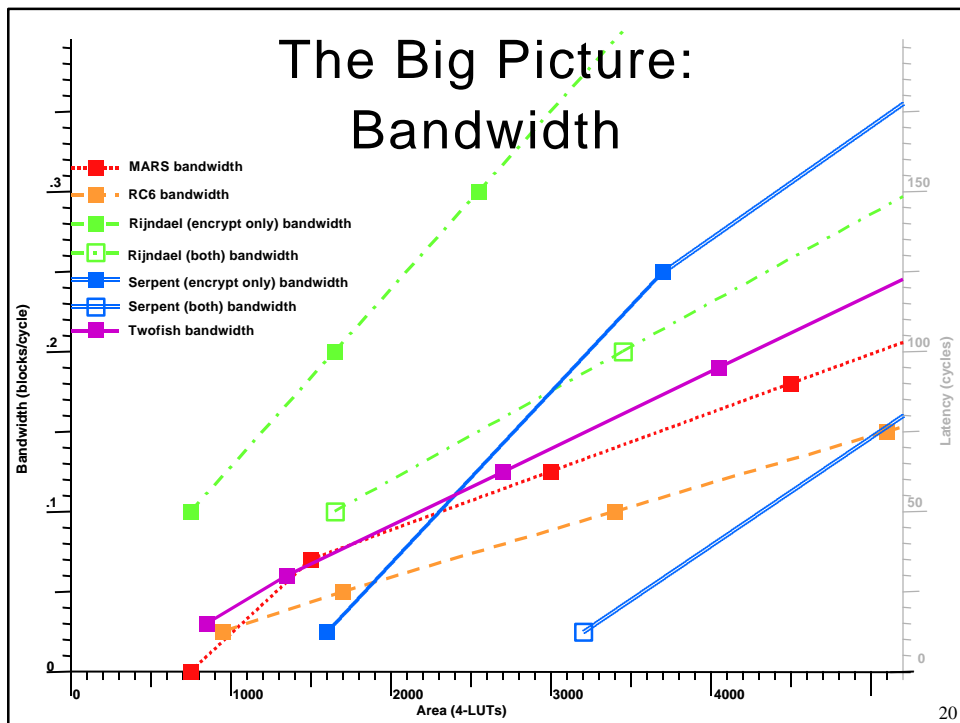
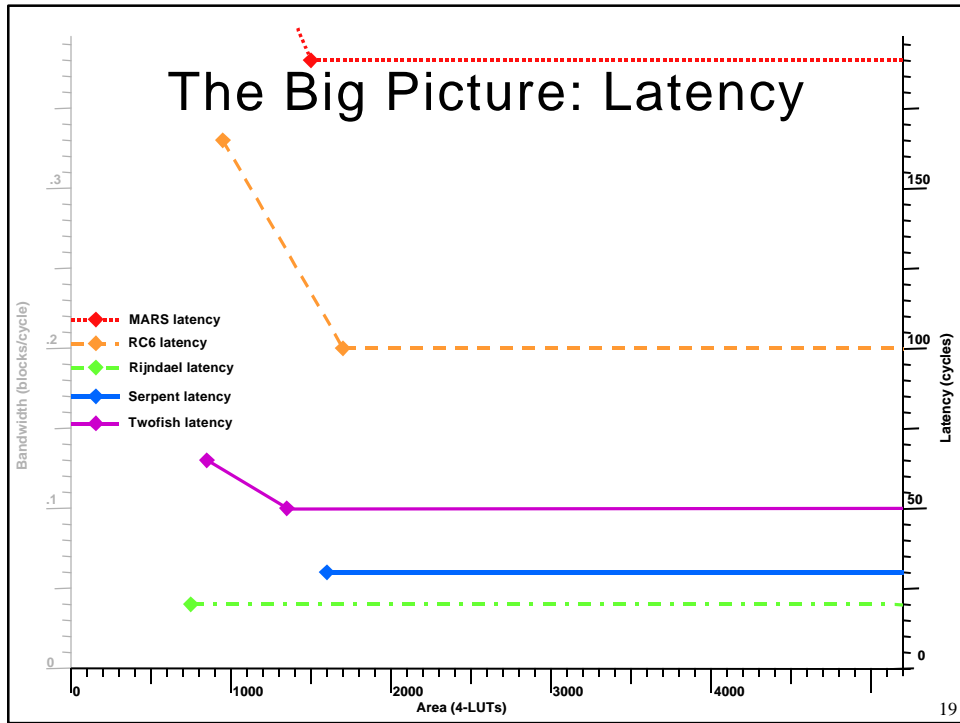


## Twofish



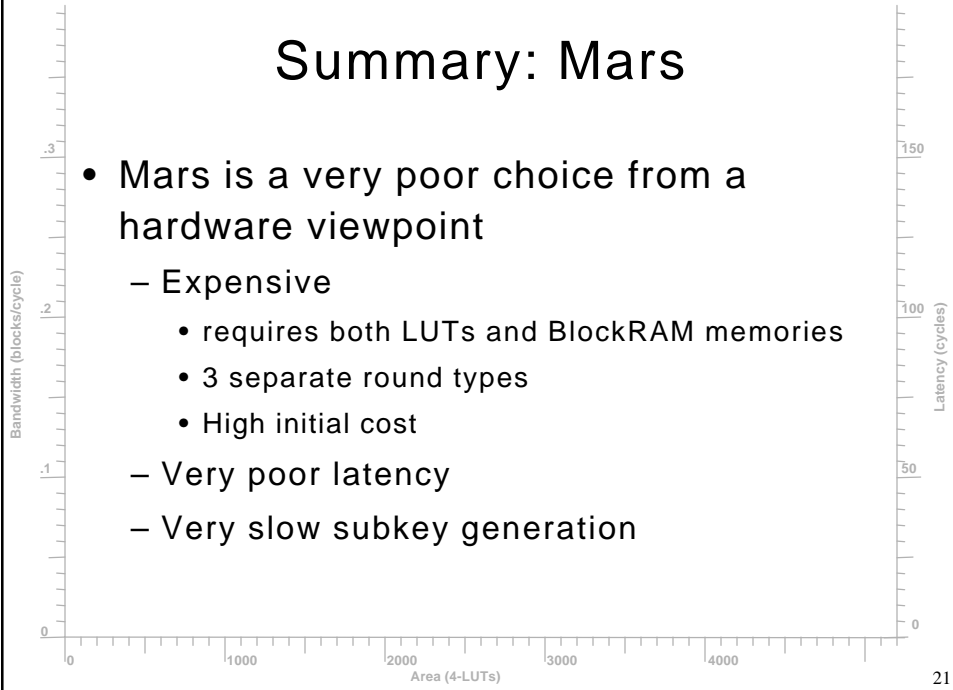
## Twofish subkey generation





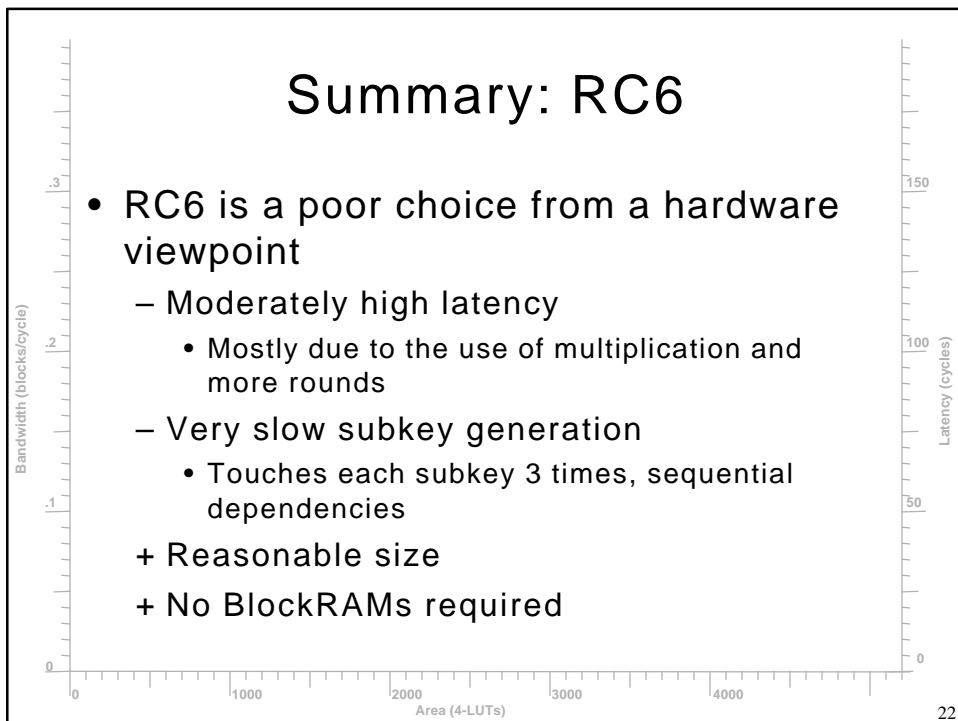
## Summary: Mars

- Mars is a very poor choice from a hardware viewpoint
  - Expensive
    - requires both LUTs and BlockRAM memories
    - 3 separate round types
    - High initial cost
  - Very poor latency
  - Very slow subkey generation



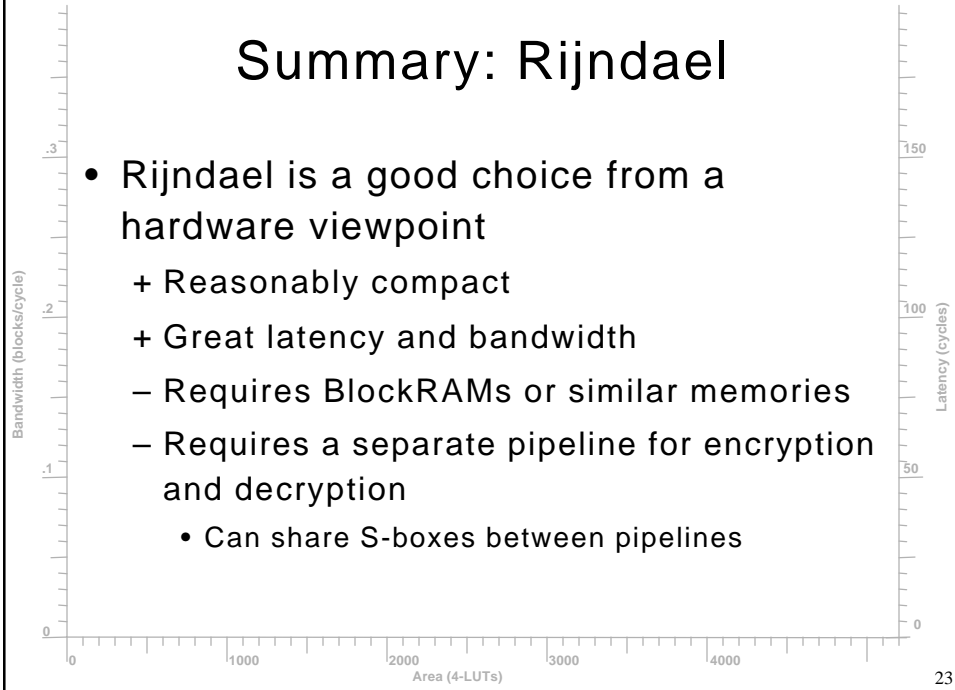
## Summary: RC6

- RC6 is a poor choice from a hardware viewpoint
  - Moderately high latency
    - Mostly due to the use of multiplication and more rounds
  - Very slow subkey generation
    - Touches each subkey 3 times, sequential dependencies
  - + Reasonable size
  - + No BlockRAMs required



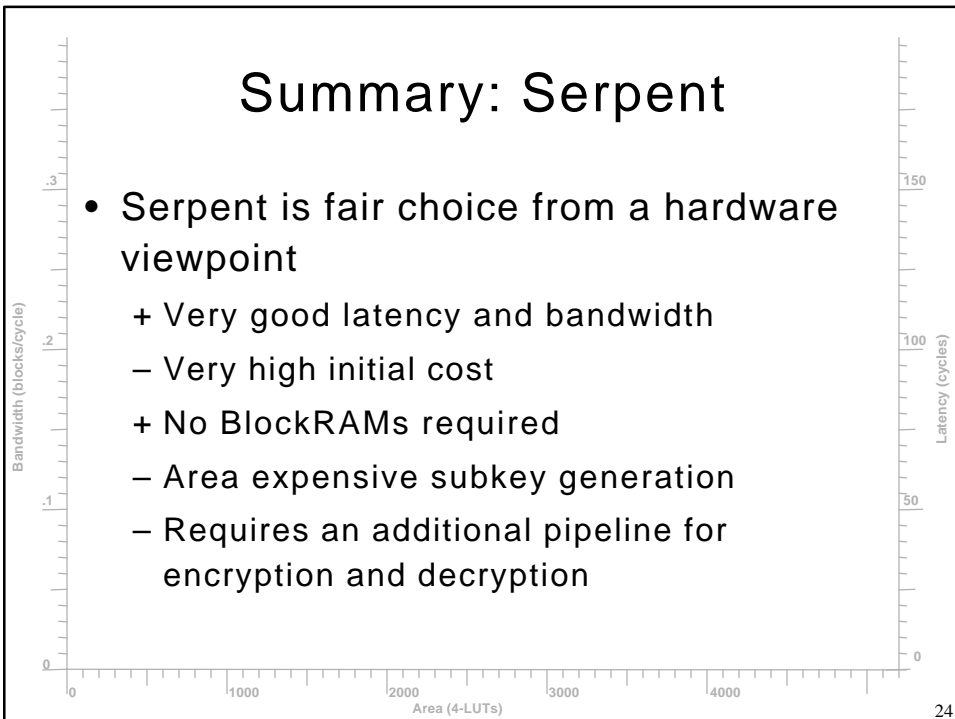
## Summary: Rijndael

- Rijndael is a good choice from a hardware viewpoint
  - + Reasonably compact
  - + Great latency and bandwidth
  - Requires BlockRAMs or similar memories
  - Requires a separate pipeline for encryption and decryption
    - Can share S-boxes between pipelines



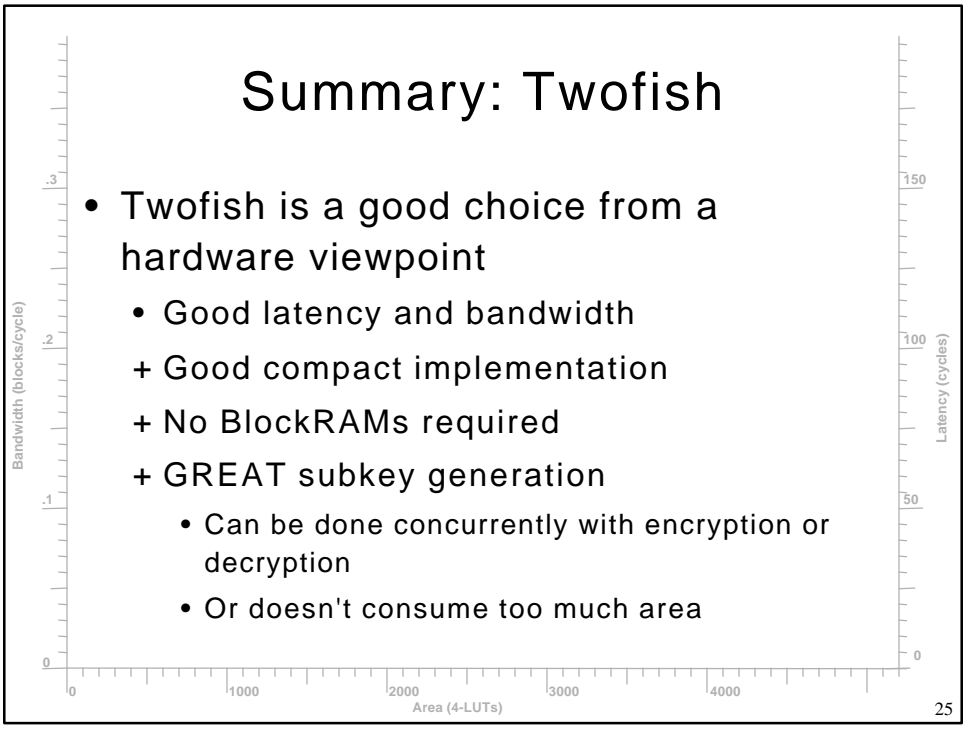
## Summary: Serpent

- Serpent is fair choice from a hardware viewpoint
  - + Very good latency and bandwidth
  - Very high initial cost
  - + No BlockRAMs required
  - Area expensive subkey generation
  - Requires an additional pipeline for encryption and decryption



# Summary: Twofish

- Twofish is a good choice from a hardware viewpoint
  - Good latency and bandwidth
  - + Good compact implementation
  - + No BlockRAMs required
  - + GREAT subkey generation
    - Can be done concurrently with encryption or decryption
    - Or doesn't consume too much area

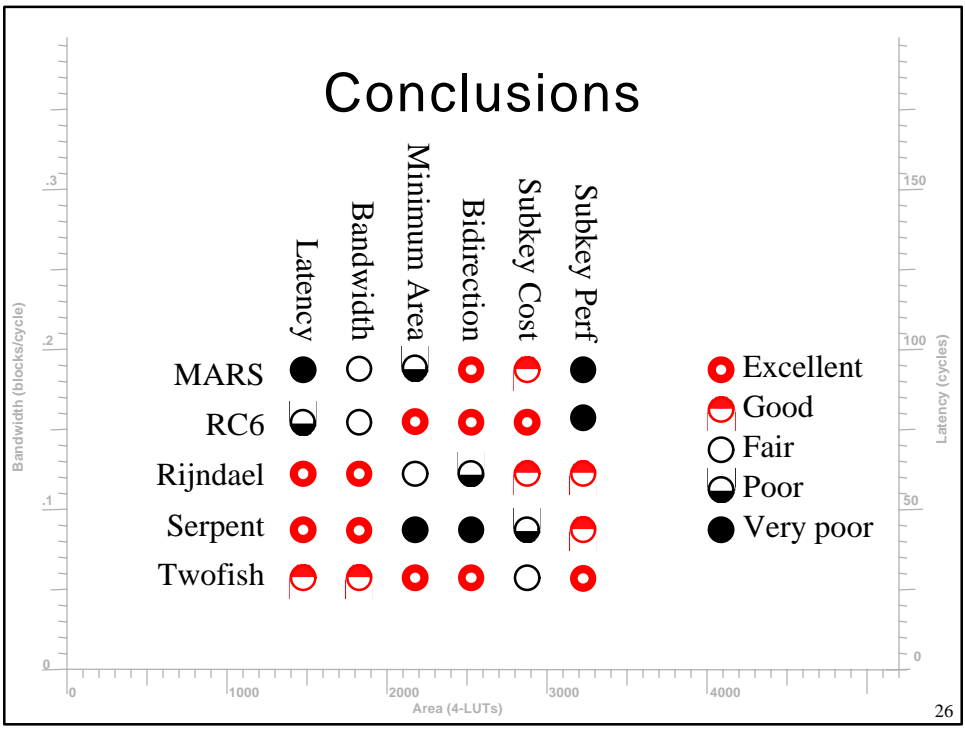


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# Conclusions

	Latency	Bandwidth	Minimum Area	Bidirection	Subkey Cost	Subkey Perf
MARS	●	○	◐	●	◐	●
RC6	◐	○	●	●	●	●
Rijndael	●	●	○	◐	◐	◐
Serpent	●	●	●	●	◐	◐
Twofish	◐	◐	●	●	○	●

- Excellent
- ◐ Good
- Fair
- ◐ Poor
- Very poor



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